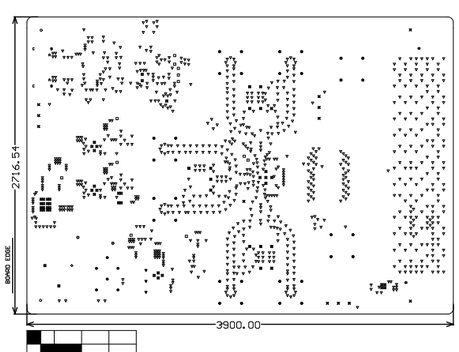
Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template	Description	Hole Tolerance (+)	Hole Tolerance (-)
◇	1	39.76mil (1.010mm)	PTH	Slot	Top Layer - Bottom Layer	Pad	Rounded	r430_170h10l_356r85			
A	2	25.59mil (0.650mm)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c65hn65m65p0			
⊠	2	29.92mil (0.760mm)	PTH	Slot	Top Layer - Bottom Layer	Pad	Rounded	r360_150h76_305r75			
✿	2	50.00mil (1.270mm)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c127hn127			
C	2	55.12mil (1.400mm)	PTH	Slot	Top Layer - Bottom Layer	Pad	Rounded Rectangle	r100_180h140_60r50m100_180p0			
O	2	63.00mil (1.600mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c221h160			
B	2	66.93mil (1.700mm)	PTH	Slot	Top Layer - Bottom Layer	Pad	Rounded Rectangle	r100_210h170_60r50m100_210p0			
✖	2	105.91mil (2.690mm)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c-127hn269			
○	2	193.86mil (3.400mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c550h340m550p0			
▼	9	42.91mil (1.090mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)			
❁	6	47.24mil (1.200mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)			
✖	10	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)			
□	12	28.00mil (0.711mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)			
✖	14	20.00mil (0.508mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v102h51e0xx0			
●	32	66.93mil (1.700mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c260h170x260p0			
⊠	44	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	(Mixed)			
▽	1008	8.00mil (0.203mm)	PTH	Round	Top Layer - Bottom Layer	(Mixed)	Rounded	(Mixed)			
	1146 Total										

Slot definitions : **Routed Path Length** = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout



Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer		1.40mil		
	Dielectric 1	FR408HR	5.00mil	3.62	
2	L2 GND	CF-004	1.40mil		
	Dielectric 3	FR408HR	3.20mil	3.46	
3	L3 PWR	CF-004	1.40mil		
	Dielectric 5	FR408HR	3.00mil	3.6	
4	L4 GND	CF-004	1.40mil		
	Dielectric 7	FR408HR	9.20mil	3.68	
5	L5 SIG	CF-004	1.40mil		
	Dielectric1	FR408HR	6.40mil	3.46	
6	L6 GND	CF-004	1.40mil		
	Dielectric 8	FR408HR	9.20mil	3.68	
7	L7 GND	CF-004	1.40mil		
	Dielectric 6	FR408HR	3.00mil	3.6	
8	L8 PWR	CF-004	1.40mil		
	Dielectric 4	FR408HR	3.20mil	3.46	
9	L9 GND	CF-004	1.40mil		
	Dielectric 2	FR408HR	5.00mil	3.62	
10	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				
Total board thickness:			62.00mil		

M10 Fab Notes

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL
MIN. CLEARANCE: 5 MIL
MIN. VIA PAD SIZE: 18 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ **HYBRID STACKUP** ☒ **UNIFORM STACKUP**
☒ ISOLA FR408HR
☐ Megtron 4 **OR** Isola I-Speed
☐ Megtron6 **OR** Isola MT-40 **OR** Nelco MW-1000
☐ OTHER _____
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER 92 MIL +/-10%
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER _____

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER _____
SOLDER RESIST COLOR: ☐ GREEN ☒ OTHER RED
☒ MATTE ☐ SEMI-GLOSS
SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ HARD GOLD (30u)
☐ OTHER _____
ARRAY/PANEL: ☒ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☐ V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

FAB INSTRUCTIONS

☒ 16 MIL & SMALLER VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☒ TOP LAYER TRACKS 9.7 MIL WIDE REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ OUTER LAYER TRACKS XX MIL WIDE WITH XX MIL SPACE REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE
☐ INNER LAYER XX & XX TRACKS XX MIL WIDE REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ INNER LAYER TRACKS XX MIL WIDE WITH XX MIL SPACE REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE
☐ NO PULL-BACK ON COPPER FEATURES TO EDGE OF THE BOARD

TEXAS INSTRUMENTS

PROJECT TITLE: ADC3644EVM
DESIGNED FOR: Public Release
FILE NAME: ADC3644EVM.PcbDoc

ENGINEER:	LAYOUT BY:
GBR	GBR
SCALE: 1.00	ALTIUM DESIGNER VERSION: 24.7.2.38

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: DC104	REV: G1	SVN REV: 361d0e17a7f126cfb2fa13855cdd4d2de4992523 [Locally Modified]
LAYER NAME = [illegible]			
PLOT NAME = Fabrication Drawing	GENERATED : 1/9/2025 4:50:35 AM	TEXAS INSTRUMENTS	

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